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## CERTIFICATE OF TRANSMISSION

**July 27, 2005**

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| **Atty Docket No.** | : | JCLA6643 |
| **Application No.** | : | 09/801,350 |
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**BY FACSIMILE ONLY**

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| **Fax No.** | : | 571-273-8300 |
| **Attention** | : | **EXAMINER : NADAV, ORI** |
| **Group Unit** | : | 2811 |
| **From** | : | Jiawei Huang, Reg. No. 43,330 |
| **MESSAGE** | : | Enclosed herewith is a Notice of Appeal in 1 page and a Pre-Appeal Brief Request for Review in 4 pages. |

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office on **July 27, 2005** at the above indicated fax number.

Sign by: _____
Jiawei Huang

**Application No.: 09/801,350** **Docket No.: JCLA6643**

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of
Applicants : Lai et al. )
Serial No. : 09/801,350 )
Filed : March 07, 2001 )
For : Electrostatic Discharge Protection )
Circuit Coupled On I/O Pad )
)

## PRE-APPEAL BRIEF REQUEST FOR REVIEW

**Mail Stop AF**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated April 27, 2005, please consider the following remarks.

**Present Status of the Application**

Claims 1-4, 13 and 15 are pending in the present application.

In the Office Action dated April 27, 2005, in rejecting claim 15 (at the last paragraph of page 6), the Examiner stated that it would have been obvious to a person skilled in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse in Quigley's device in order to improve the protection capability of the device.

Applicants respectfully disagree and would like to point out that, according to the claimed invention, the anti-latch-up circuit is connected to the SCR circuit and the SCR circuit is connected to the I/O pad. The anti-latch-up circuit is designed to prevent activation of the SCR circuit during the normal IC operation. The claimed invention proposes setting a RC DELAY TIME of the anti-latch up circuit smaller than a voltage

rising time of the IC power but greater than the voltage rising ESD pulse (as specified in claim 15). Accordingly, when there is an accidental over-voltage or voltage surge during the normal IC operation, because the RC Delay Time of the anti-latch up circuit is designed to be smaller than a voltage rising time of the IC power, therefore the rising voltage of the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power so that a voltage level of the node A has the same voltage (Vdd). Thus, a large amount of carriers, due to accidental over voltage, may be accordingly absorbed and the latch-up phenomenon is avoided. On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, therefore the rising voltage of the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit. Therefore the SCR circuit may be triggered at a lower holding voltage.

Instead, Quigley, at col. 5, lines 1-4, substantially teaches to sufficiently prolong the delay time of the SCR to prevent normal signals of the integrated circuit from triggering the SCR.

Furthermore, Quigley, at col. 4, lines 41-62, substantially teaches that because gate oxide breakdown occurs when a 10 volt DC voltage is applied across the gate oxide or a 20 volt transient voltage, and therefore ESD protection circuit 11 must enable SCR 22 before the pad reaches 20 volts because an ESD event is a transient phenomenon corresponding to the higher voltage for gate oxide breakdown. Thus, Quigley substantially proposes setting a threshold voltage of, for example, 12 volts, as trigger voltage at the pad, and when the voltage at the pad exceeds 12 volts, the SCR circuit is triggered. Quigley utilizes a voltage divider circuit, including a capacitor 17 and a resistor 18, designed for generating a control voltage to SCR 22 due to a transient voltage applied to the pad when the voltage at the pad exceeds threshold voltage 12 volts.

Therefore, it is clear that the mechanism of preventing triggering and triggering of the SCR of the claimed invention is substantially different from that of Quigley, in that

the claimed invention does not prolong the delay time of the SCR to prevent normal signals of the IC from triggering the SCR or set any threshold voltage for triggering the SCR as expressly taught by Quigley, instead the claimed invention proposes designing the RC Delay Time of the anti-latch-up circuit to be smaller than the voltage rising of the IC power but greater than the rising voltage time of the ESD pulse so that the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power to prevent triggering the SCR, and during the ESD event, the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit.

Accordingly, Applicants respectfully submit that Quigley cannot possibly suggest one skilled in the art to modify Quigley's ESD device in a manner suggested by the Examiner because any such modification of Quigley's device would frustrate its intended purpose. As such, Quigley is complete and functional by itself, so there would be no reason to modify ESD circuit of Quigley, and certainly not to modify the voltage divider of Quigley in the manner suggested only by the Examiner. Applicants respectfully submit that it is impermissible, however simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from references to fill the gaps, and any such reconstruction to depreciate the claimed invention would be construed as hindsight reconstruction.

Furthermore, Applicants respectfully submit that Lin substantially teaches that the voltage transition circuit (51) is adapted to provide a voltage transition such that the P+/n well junction of the SCR is forward biased a number of times during early stage of an ESD event. According to Lin, the voltage transition provided by the voltage transition circuit (51) has ramp rate faster than the ESD voltage's ramp rate. Therefore, it clear that Lin substantially fails to teach, suggest or hint that the anti-latch-up circuit has a RC delay time that is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as required by the dependent claim 15, instead, Lin substantially teaches the voltage transition provided by the voltage transition circuit (51)

has a ramp rate faster than the ESD voltage's ramp rate. In other words, because Lin substantially teaches the voltage transition has RC delay time SMALLER THAN the ESD VOLTAGE'S RAMP RATE, therefore, it is clearly evident that Lin substantially teaches away from the claimed invention in this regard.

Accordingly, for at least the foregoing reason, Claim 15 patently defines over Quigley and Lin and therefore Claim 15 should be allowed.

Furthermore, Applicants respectfully submit that both Quigley and Lin fails to teach, suggest or hint a SCR circuit connected to the I/O pad and an anti-latch-up circuit comprising a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit as required by Claim 1. In other words, the anti-latch-up circuit is directly connected to the SCR circuit but NOT directly connected to the I/O pad (please see FIG. 4).

Instead, Quigley, in FIG. 1, substantially discloses that BOTH the voltage divider (17, 18) and SCR circuit 22 are directly connected to the I/O pad. Likewise, Lin, in FIG. 5, also substantially discloses BOTH the transient generator 51 and SCR circuit are connected to the I/O pad or the VDD bus. Accordingly, for at least the foregoing reason, Claim 1 patently defines over Quigley and Lin and therefore Claim 1 should be allowed.

Respectfully submitted,
J.C. PATENTS

Date: 7/27/2005

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